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20ELD21

Second Semester M.Tech. Degree Examination, July/August 2022
Advanced Computer Architecture

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Describe the shared memory multiprocessor models. **(06 Marks)**

b. List the performance factors and system attributes. Explain how performance factors are influenced by system attributes. **(08 Marks)**

c. Explain the architecture of vector super computer. **(06 Marks)**

OR

2 a. Define the types of data dependence. Also compute the dependence graph for the following code segment :

S1 : load R1, A
S2 : Add R2, R1
S3 : Move R1, R3
S4 : Store B, R1 **(10 Marks)**

b. Demonstrate the mismatch between software and hardware parallelism in the following program graph given in Fig Q2(b). Also show that how will it be matched by using dual processor system

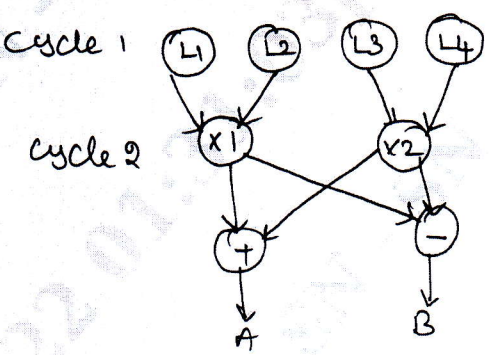

Fig Q2(b)

L_i = load operation
X_i = Multiply operation **(10 Marks)**

Module-2

3 a. Briefly explain the virtual memory models for multiprocessor system. **(06 Marks)**

b. With neat diagram, explain the hierarchical memory technology. **(06 Marks)**

c. Explain VLIW processor architecture and its pipeline operation. **(08 Marks)**

OR

4 a. Explain mean performance of a multimode computer. **(04 Marks)**

b. Explain the following parameters used for evaluating parallel computation. **(06 Marks)**
i) System efficiency ii) Redundancy and utilization iii) Quality of parallelism.

c. Explain any two speed up performance models in detail. **(10 Marks)**

Module-3

5 a. Explain sequential and weak consistency models. **(06 Marks)**

b. Illustrate daisy – chained and distributed arbitration techniques. **(08 Marks)**

c. Explain Direct mapping cache organization. **(06 Marks)**

OR

6 a. Explain multiply pipeline design to multiply two 8-bit integers.
X = 1011 0101 Y = 1001 0011 **(10 Marks)**

b. Explain the mechanism of instruction pipelining. **(10 Marks)**

Module-4

7 a. With diagram, explain the architecture of the connection machine CM – 2. **(10 Marks)**

b. Explain four context switching policies. **(04 Marks)**

c. Explain briefly different vector access memory schemes. **(06 Marks)**

OR

8 a. Explain in detail the Stanford Dash prototype system with diagram. **(10 Marks)**

b. Explain the following with respect to latency hiding techniques.
i) Shared virtual memory ii) Perfecting techniques. **(10 Marks)**

Module-5

9 a. Explain the fairness policies and sole access protocols in the principle of synchronization. **(10 Marks)**

b. Explain the compilation phases in parallel code generation. **(10 Marks)**

OR

10 a. Discuss shared variable program structure. **(10 Marks)**

b. Explain the language features for parallelism. **(10 Marks)**

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